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Please replace the paragraph at page 22, lines 3-8 with the following amended paragraph:

FIG. 6G illustrates the formation of a Si₃N₄ layer 110 on the wafer. FIG. [6G] <u>6H</u> also illustrates that the substrate 10 may be thinned as described above to provide a thinned substrate 10'. The metallization 32 may then be formed on the thinned substrate 10' as illustrated in FIG. 6I. Contact holes may also be formed through the Si₃N₄ layer 110 so as to allow contact between the source, drain and gate contacts and a metallized interconnect layer (not shown).